(Amended) 2. The method of manufacturing a semiconductor device according to claim 1, wherein said doping step comprise implanting ions of an impurity.

(Amended) 5. The method of manufacturing a semiconductor device according to claim 1, wherein the step of forming said gate oxide layer forms the gate oxide layer of transistors driven at said first voltage and the transistors driven at said second voltage.

(Amended) 6. The method of manufacturing a semiconductor device according to claim 1, wherein the gate electrode of transistors driven at said first voltage are doped at said first concentration, and the gate electrode of transistors driven at said second voltage are doped at said second concentration.

REMARKS/ARGUMENTS

Claims 1, 2, 5, and 6 remain in the application. Claims 3, 4, 7, and 8 have been canceled hereby without predjudice. Applicant reserves the right to pursue the original claims and the other claims in this application and in other applications.

Examiner has indicated that Applicant has not filed a certified copy of the Japanese application as required by 35 U.S.C. § 119(b). Note, the Applicant has filed a certified copy of the priority application in the parent application, Serial No. 09/021,519 filed February 10, 1998 and Examiner is respectfully requested to refer to the parent application for the certified copy.

The Information Disclosure Statement filed June 4, 2001, is objected to as failing to comply with 37 C.F.R. §1.98(a)(2). In accordance with 37 CFR §1.98(d), copies of the listed references that were previously cited by or submitted to the U. S. Patent and Trademark Office in the parent application 09/021,519 filed February 10, 1998 are not included here. The Examiner is respectfully requested to refer to the parent

application for any copies of the references.

Claims 1-8 are rejected under 35 U.S.C. §103(a) over Tigelaar et al. (U.S. patent 5,595,922) in view of Wolf "Silicon Processing for the VLSI Era Volume 2: Process Integration."

The present invention is directed to a method of manufacturing a multi-voltage level semiconductor device including; Independent Claim 1 explicitly requires:

> *masking a portion of said plurality of active regions*; and
>
> doping an unmasked portion of said plurality of active regions at a second concentration higher than the first concentration with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level.

In other words, a first doping is performed with an impurity at a first concentration to all the active regions, a portion of the active regions are then masked and a second doping is performed with an impurity at a second concentration, higher than the first concentration in the unmasked portions. In an exemplary embodiment of the present invention, the doping may be performed by ion implantation. In this way, the active regions subjected to the double ion implantation (high impurity concentration) will form transistors adapted for low voltage operation and those active regions, which are masked, and are subjected to only one ion implantation will form transistors adapted for high voltage use. See Applicant's specification pages 7-10.

In this way, as shown in Fig. 1C, when a power supply voltage is applied to the gate electrode 4b, an inverse bias acts between the source region 5b, channel region 7b and gate electrode 4b, thereby creating a depletion layer DP. The gate electrode 4b effectively develops a boundary, as marked by the dotted line, and the effective position of the gate electrode 4b in the lowermost portion thereof moves from "X" to "Y". Hence, when a high voltage is applied to the gate electrode of a high-voltage circuit MOS transistor, the

electric field applied to the gate oxide film is reduced by the depletion layer created in the gate electrode 4b, and breakdown voltage is thereby improved.

Similarly, as shown in Fig. 1D, the source region 5a is constituted by an extended section (LDD region) 10 of low impurity concentration, which partially overlaps with the gate electrode 4a in the plane of the substrate, and a source region 11 of high impurity concentration, which is aligned with the edge of the insulating spacer 9. The high-impurity-concentration source region 11 lowers the effective resistance of the source region. Also, since the gate electrode 4a is doped with impurity at a high concentration, no depletion layer is created. Hence, by selecting an optimum thickness of the gate oxide film 3 for the low-voltage MOS transistor, a high-performance low-voltage MOS transistor can be formed.

Tigelaar, as indicated in the Office Action, does not show the doping/masking steps as claimed. However, Examiner proposes that Wolf remedies the deficiency, namely, Examiner indicates that Wolf teaches that it is conventional to have drain structures in MOS devices and that LDDs are used to absorb some of the potential into the drain and reduce the maximum electric field (E_m). Hence, Examiner indicates that it would have been obvious to combine the teachings of Tigelaar with that of Wolf. Applicant respectfully disagrees.

As noted above, the present invention is directed to a method of fabricating a multi-voltage level device. Specifically, the method provides, at least, doping with an impurity a plurality of active regions "at a first concentration," then masking "a portion" of the plurality of active regions and doping an unmasked portion "at a second concentration higher than the first concentration" with an impurity to form the multi-voltage level devices, as recited in independent Claim 1. The teachings of Wolf is simply a prior art method of forming LDDs. Wolf is completely void of any disclosure relating to, at least, the steps as described above to form a multi-voltage level device. Hence, the cited references either alone or in combination does not disclose or suggest the claimed invention.

Claims 2, 5 and 6 depend from Claim 1 and should be allowable, along with Claim 1, for the same reasons as described above, and others. Claims 3, 4, 7 and 8 have been canceled and the rejection as to these claims are rendered moot.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Attached hereto is a marked-up version of the changes made to the specification, abstract and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Dated: March 12, 2002

Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

In the Specification:

Please amend the specification as follows:

On page 1, beneath the title:

This application is a divisional of 09/021,519 filed on February 10, 1998, now U.S. Patent No. 6,271,572 which is based on Japanese patent application No. 9-28132 filed on February 12, 1997, the whole contents of which are incorporated herein by reference.

In the Claims:

Please amend the claims as follows:

(Amended) 1. A method of manufacturing a semiconductor device comprising a plurality of multi-voltage level MOS transistors comprising [the steps of]:

[preparing] providing a semiconductor substrate having a plurality of active regions of a first conductivity type;

forming [first] a gate oxide [films] layer having a first thickness onto said plurality of active regions;

forming an electrode layer onto said [first] gate oxide [films] layer;

patterning said electrode layer to form a gate electrode [patterns] onto each of said plurality of active regions:

oxidizing [the surface] a sidewall of said gate electrode [patterns] to form [second] on said oxide [films] layer a second thickness greater than said first thickness [which is integrated with said first gate oxide films, and gradually decrease

in thickness] from said sidewall[s] of the gate electrode [pattern] towards a centre portion thereof;

[first] doping said plurality of active regions at a first concentration with an impurity of a second conductivity type which is opposite to said first conductivity type using said gate electrode [patterns] as a mask[,] to form a first transistor driven at a first voltage level [to dope said gate electrode patterns and the active regions on either side thereof at low concentration]; [and]

forming spacers on said sidewall of said gate electrode;

masking a portion of said plurality of active regions; and

[second] doping an unmasked [, while covering a] portion of said plurality of active regions [by a mask, remainder of the active regions] at a second concentration higher than the first concentration with an impurity of [a] said second conductivity type[,] to [dope the gate electrode patterns and the active regions on either side thereof at the second concentration in said remainder of the active regions] form a second transistor driven at a second voltage level lower than said first voltage level.

(Amended) 2. The method of manufacturing a semiconductor device according to claim 1, wherein said [first doping step and said second] doping step comprise [a step of] implanting ions of an impurity.

(Amended) 5. The method of manufacturing a semiconductor device according to claim [4] 1, wherein the step of forming said [first] gate oxide [films] layer forms the gate oxide [films] layer of the [MOS] transistors driven at said [second] first voltage and the [MOS] transistors driven at said [first] second voltage [commonly in same processing step].

(Amended) 6. The method of manufacturing a semiconductor device according to claim [5] 1, wherein the gate electrode [patterns] of [MOS] transistors driven at said [second] first voltage are doped at [a] said first concentration, and the

gate electrode [patterns] of [MOS] transistors driven at said second [relatively low] voltage are doped at [a] said second concentration.